Claims

What is claimed is:

[c1] An integrated circuit, comprising:

a clock driver disposed on the integrated circuit;

a clock grid disposed on the integrated circuit; and

at least one interconnect connecting an output of the clock driver to the clock grid at a connection point, wherein the connection points resides at a non-peripheral region of the clock grid.

[c2] The integrated circuit of claim 1, wherein the connection point is positioned such that a component operatively connected to the clock grid at the connection point receives a signal from the clock driver at the connection point, where the signal at the connection point has less skew than if the connection point was positioned at a peripheral region of the clock grid.

[c3] The integrated circuit of claim 1, wherein the at least one interconnect is arranged in a wire tree configuration.

[c4] The integrated circuit of claim 3, wherein the wire tree configuration is balanced.

[c5] A computer system, comprising:

an integrated circuit having a clock grid;

at least one clock driver that provides a clock signal to the clock grid; and

a transmission structure operatively connecting an output of the at least one clock driver to at least one point on the clock grid, wherein the at least one point resides at a non-exterior region of the clock grid.

[c6] The computer system of claim 5, wherein the at least one point is positioned such that a component operatively connected to the clock grid at the at least one point

receives a signal from the clock driver at the at least one point, where the signal at the at least one point has less skew than if the at least one point was positioned at an exterior region of the clock grid.

[c7] The computer system of claim 5, wherein the transmission structure has a wire tree configuration.

[c8] The computer system of claim 7, wherein the wire tree configuration is balanced.

[c9] A method for reducing clock skew, comprising:

sending a clock signal from a clock driver to a first component through a connection point on a clock grid; and

sending the clock signal from the clock driver to a second component through the connection point,

wherein the connection point is at a non-peripheral region of the clock grid.

[c10] The method of claim 9, wherein the clock signal received by the first component and the second component has less skew than if the connection point was at a peripheral region of the clock grid.

[c11] The method of claim 9, wherein sending the clock signal from the clock driver to the first component and the second component occurs through a transmission structure, wherein the transmission structure comprises interconnect that connect the clock driver to the connection point on the clock grid.

[c12] The method of claim 11, wherein the transmission structure is balanced.

[c13] A transmission structure for driving a signal onto a clock grid, comprising:

an interconnect connecting a clock driver to the clock grid,

wherein the interconnect connects the clock driver to the clock grid at a connection point residing at a non-exterior region of the clock grid.

[c14] The transmission structure of claim 13, wherein the transmission structure is balanced.